Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **RIN 1 -**
2. **RIN 1 +**
3. **ROUT 1**
4. **EN**
5. **ROUT 2**
6. **RIN 2 +**
7. **RIN 2 -**
8. **GND**
9. **GND**
10. **RIN 3 -**
11. **RIN 3 +**
12. **ROUT 3**
13. **EN +**
14. **ROUT 4**
15. **RIN 4 +**
16. **RIN 4 -**
17. **VCC**
18. **VCC**

**2 1 18 17 16**

**15**

**14**

**13**

**12**

**3**

**4**

**5**

**6**

**7 8 9 10 11**

**.060”**

**.061”**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: FLOATING**

**Mask Ref: B**

**APPROVED BY: DK DIE SIZE .060” X .061” DATE: 8/1/16**

**MFG: NATIONAL THICKNESS .016” P/N: DS90C032C**

**DG 10.1.2**

#### Rev B, 7/1